TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION VII
MCS-RAM 16K PC BOARD
TEI INC.

P/N 13686-7

TEI, INC. 16K RAM BOARD -4200 STATIC RANDOM ACCESS MEMORY-
DESIGNED FOR THE S100 BUS
LOW POWER - NO WAIT STATES
8080 OR Z80

EMM/SEMI 4200 RAM CHIPS ARE ORGANIZED IN AN ARRAY OF 64 ROWS BY 64 COLUMNS (4096 X 1 BIT). WHEN CHIP SELECT IS HIGH ALL PINS ARE IN AN INOPERATIVE HIGH IMPEDANCE STATE, AND POWER IS SUPPLIED ONLY TO THE MEMORY ELEMENTS. THE MEMORY CELLS (BECAUSE THEY ARE CROSS COUPLED HIGH IMPEDANCE STATIC CELLS) WILL RETAIN DATA DOWN TO Vdd = 4 VOLTS DC. THE NORMAL VOLTAGE LEVEL FOR Vdd IS 12 VOLTS DC. THERE IS AN APPROXIMATE 10 TO 1 REDUCTION IN POWER CONSUMPTION DURING THE ACTIVE TO STANDBY MODE OF OPERATION. DATA WILL BE VALID EXCEPT FOR THE MOST SEVERE BROWN-OUT CONDITIONS.

THE 4200 CHIP REQUIRES 3 SUPPLY VOLTAGES +5, -5, AND +12 VDC. DUE TO BOARD ORGANIZATION, ONLY ONE 4K BLOCK OF RAM AT ANY GIVEN TIME IS ACTIVE IN SYSTEM MEMORY RESULTING IN EXTREMELY LOW POWER CONSUMPTION. THIS GREATLY EASES SYSTEM GENERATED HEAT AND POWER LOSS. TYPICALLY RAM IS THE LARGEST CURRENT DEMAND IN ANY GIVEN SYSTEM.

FEATURES:

S-100 BUS 4MHz OPERATION
VERY LOW POWER 620MA +5 320MA +12 96MA -5
SOLDER MASK SILK SCREEN PLATED THROUGH HOLES

EACH 4K BLOCK ADDRESSABLE TO ANY 4K BOUNDARY
EACH 16K CARD ADDRESSABLE TO ANY ONE OF 16 PAGES

A TOTAL OF 256K MAY BE ADDRESSED TO THE SAME LOCATION
64 4K BLOCKS MAY BE ADDRESSED TO THE SAME LOCATION

FULLY BUFFERED
BOARD WILL ALSO SUPPORT NEC 410 MEMORY CHIPS.
PHANTOM PIN 67 OF S-100 BUS IMPLEMENTED.

FUNCTIONAL DESCRIPTION:

ADDRESS SELECT

EACH 4K BLOCK IS REPRESENTED BY P0, P1, P2, AND P3.

MEMORY ADDRESSES ARE IN INCREMENTS OF 4K BLOCKS. BY JUMPERING P0 TO BLOCK 0 SETS THE FIRST 4K BLOCK TO MEMORY LOCATION 0000 HEX. P1 TO 4 SETS THE NEXT 4K BLOCK TO MEMORY LOCATION 4000 HEX. P2 TO 8 SETS THE NEXT 4K BLOCK TO MEMORY LOCATION 8000 HEX. P3 TO 12 SETS THE NEXT 4K BLOCK TO MEMORY LOCATION 6000 HEX - ENDING AT 7FFF HEX. THIS BOARD NOW OCCUPIES THE FIRST 16K OF RAM 0000 - 3FFF HEX.

THE ABOVE EXAMPLE ASSUMES THAT PAGE SELECT IS IN THE DEFAULT MODE P0, P1, P2, AND P3 MAY BE JUMPERED TO ANY ONE OF 16 POSITIONS (0,4,8,12,16,20, 24,28,32,36,40,44,48,52,56,60) WHICH COVERS THE NORMAL RANGE OF 0 TO 64K.

ADDRESS SELECT	HEX ADDRESS		
0	0000	0FFF	
4	1000	1FFF	
8	2000	2FFF	
12	3000	3FFF	
16	4000	4FFF	
20	5000	5FFF	
24	6000	6FFF	
28	7000	7FFF	
32	8000	8FFF	
36	9000	9FFF	
40	A000	AFFF	
44	B000	BFFF	
48	C000	CFFF	
52	D000	DFFF	
56	E000	EFFF	
60	F000	FFFF	TOP OF MEMORY 64K

THE DECODE CHIP FOR THE ABOVE ADDRESS IS A 74154. THIS IS A 1 OF 16 DECODE CHIP WHICH LOOKS AT THE HIGH ORDER 4 BITS AND DETERMINES WHICH 4K BLOCK IS BEING ADDRESSED BY THE MICROPROCESSOR. IC 40 A 7474 FLIP-FLOP, SUPPLYS THE NECESSARY TIMING FOR THE 4200 CHIP BY DECODING PSYNC, PHASE 1 CLOCK, AND IS RESET BY SMEMR. IC 49 AND IC 35 SERVE TO CREATE THE ON-CARD READ WRITE SIGNAL, AND TO EXTEND THE ADDRESS DECODE ENABLE SIGNAL CREATED BY THE 7474 FLIP-FLOP. THE IN916 DIODE IS USED TO INSURE THAT DURING A MEMORY READ THE DATA OUT (MEMORY BOARD) BUFFER IS IN CONTROL OF THE CHIP ENABLE FOR ADDRESS DECODE UNTIL THE ADDRESS BUS GOES NOT TRUE. ONCE A READ CYCLE IS STARTED IT IS KEPT ACTIVE UNTIL THE ADDRESS BUS BIT PATTERN CHANGES STATE.

IC 46 AND 39 (SMEMR AND POBIN) IS USED TO CREATE THE ON CARD MEMORY READ SIGNAL. IF MEMORY READ IS TRUE (ACTIVE LOW) AND ADDRESS DECODE IS TRUE AND PAGE SELECT IS TRUE THEN A MEMORY READ IS ACTIVATED.

WHEN MEMORY WRITE (BUS SIGNAL M WRITE-PIN 68) IS TRUE, AND ADDRESS DECODE IS TRUE, AND PAGE SELECT IS TRUE THEN A MEMORY WRITE IS ACTIVATED. DURING THIS MODE THE 7474 FLIP-FLOP IS NOT THE PRIMARY SIGNAL SOURCE FOR THE FUNCTION.

PAGE SELECT

IC 44 (74154) IS USED FOR PAGE SELECT. THIS IS A ONE OF SIXTEEN DECODE CHIP. DATA TO BE DECODED IS STORED IN A SINGLE 74175 (LATCH) BY OUT-PUTTING TO PORT 7F (HEX). ONLY THE UPPER 4 BITS ARE USED TO CONTROL THE PAGE SELECT. PAGE ZERO IS THE DEFAULT MODE AS SHIPPED FROM THE FACTORY. IC 41 (74LS30) DECODES THE LOWER 8 BITS OF THE ADDRESS BUS AND WHEN BUS SIGNAL "SOUT" AND "PWR" ARE TRUE DATA IS LATCHED INTO THE 74175.

EXAMPLE BIT PATTERNS FOR PAGE SELECT

PAGE SELECTED	BIT 7	BIT 6	BIT 5	BIT 4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	0	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

FOR THE ABOVE PAGE SELECTION BIT CODES THE PAGE SELECT JUMPERS P0, P1, P2, AND P3 ARE IN THE DEFAULT MODE. JUMPER P0 TO P1 TO P2 TO P3 TO NP ---- NP THEN JUMPERS TO ONE OF THE 16 DECODE BITS OF THE 74154 LABELED 0 THRU 15.

NOTE: THE JUMPER LABELED 16K ALSO MUST BE JUMPERED. THIS IS THE MODE AS SHIPPED FROM THE FACTORY. NP IS JUMPERED TO DECODE BIT 0. SEE SCHEMATIC DRAWING 13564.

BANK/PAGE SELECT

IC 42 (74175) IS USED TO LATCH IN THE LOWER 4 BITS OF THE DATA BUS IN THE SAME MANNER THAT IC 43 ABOVE FUNCTIONS USING PORT 7F (HEX). THE PURPOSE OF THE 4 BITS IS TO CONTROL WHICH OF THE 4 4K BLOCKS OF RAM IS TO BE ACTIVE WHEN THE JUMPERS LABELED PAGE SELECT ARE JUMPERED TO THE 74175 (IC 42). THIS OPTION ALLOWS THE USER TO JUMPER ALL 4 4K BLOCKS OF MEMORY TO THE SAME 4K ADDRESS IN SYSTEM MEMORY AND THEN USE THE ONE OF SIXTEEN DECODER (BANK SELECT) AND PAGE SELECT THRU THE LOW ORDER 4 BITS TO SELECT ANY ONE OF 64 4K BLOCKS OF MEMORY ADDRESSED TO THE SAME LOCATION IN MEMORY. SINCE 64 COMBINATIONS IS QUITE LENGTHLY, NO EXAMPLE IS GIVEN.

IC 38 IS USED TO DECODE ADDRESS TRUE AND PAGE/BANK SELECT TRUE.

IC 37 DETECTS ONE OF 4 CHIP SELECT SIGNALS AND WHEN ANDED WITH MEMORY READ GATES DATA ONTO THE DATA BUS FOR A READ MODE.

IC 35 CONVERTS THE TTL SIGNAL TO THE 0 TO 12 VOLT SIGNAL NEEDED FOR THE 4200 RAM CHIP SELECT. CHIP SELECT IS ACTIVE LOW.

IC 47 AND 48 ARE ADDRESS BUS BUFFERS TO ISOLATE THE BOARD FROM THE SYSTEM BUS.

IC 49 AND 50 ARE USED TO BUFFER THE INCOMING DATA FROM THE SYSTEM BUS.

IC 36 AND 51 ARE USED TO BUFFER THE DATA OUT TO THE SYSTEM BUS (DRIVER).

TEI INC.

PARTS LIST

MCS-16K RAM

4200 SERIES

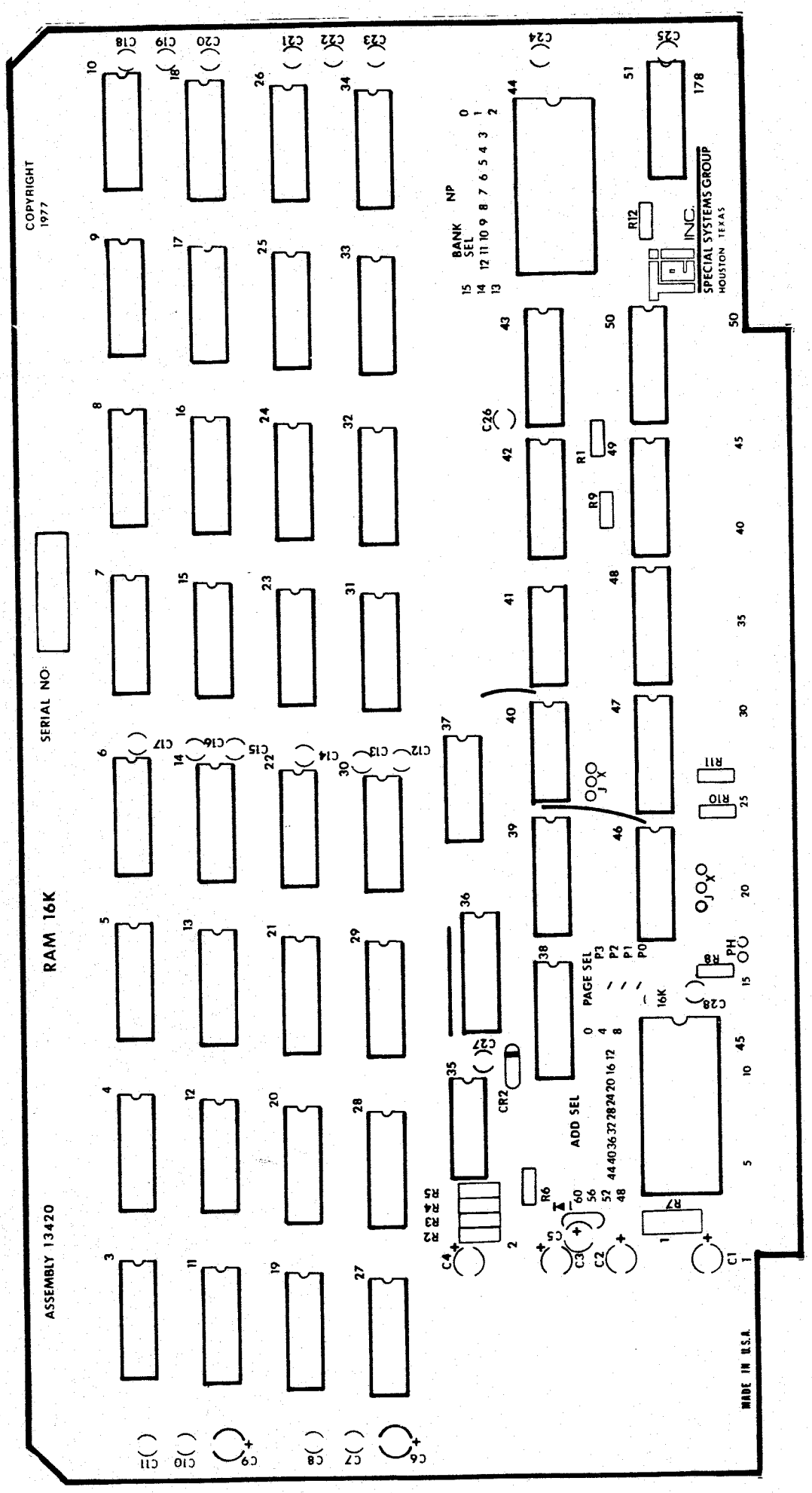
REF DES	DESCRIPTION	TEI P/N
C1 Thru C6		
C9, C25	Cap. 10MF, 20 VDC	1580-001
C7,8, C10 Thru 24		
C26,27,28	Cap, .1MF	1562-002
CR1	Diode IN 751A	4840-004
CR2	Diode In 916	4825-009
R1	RES 150 Ω 1/4 W 2%	4741-258
R2 Thru R5		
R9,R12	RES 390 Ω 1/4 W 2%	4741-298
R6	RES 910 Ω 1/4 W 2%	4741-333
R7	RES 330 Ω 1/2 W 10%	4725-291
R8	RES 4.7K 1/4 W 2%	4741-402
R10,R11	RES 130 Ω 1/4 W 2%	4741-252
U1	Regulator 7805	3120-003
U2	Regulator 7812	3120-007
U3 Thru		
U34	IC Chip RAM 4200	3163-003
U35	IC Chip 7406	3161-028
U36, U46,		
U51	IC Chip 74LS368	3164-029
U37	IC Chip 74LS21	3164-026
U38	IC Chip 74LS32	3164-027
U39	IC Chip 7432	3161-006
U40	IC Chip 7474	3161-020
U41	IC Chip 74LS30	3164-005
U42, U43	IC Chip 74175	3161-027
U44, U45	IC Chip 74L154*	3166-002
U47 Thru		
U50	IC Chip LS367	3164-028
	Heat Sink	4890-002
	PCB FAB	13421

*U44, U45 Substitute: 74LS154 3164-008

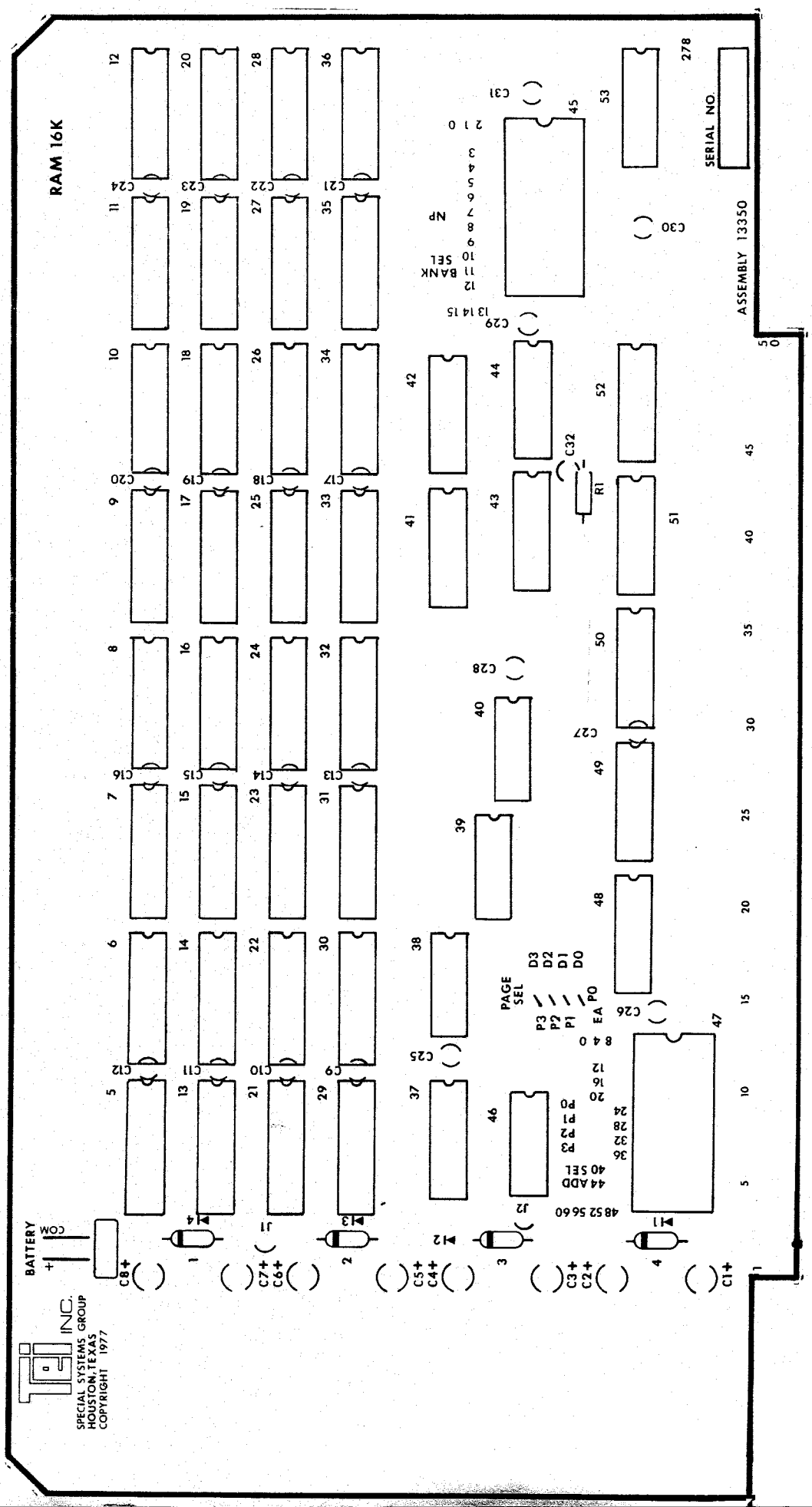
6104 SERIES

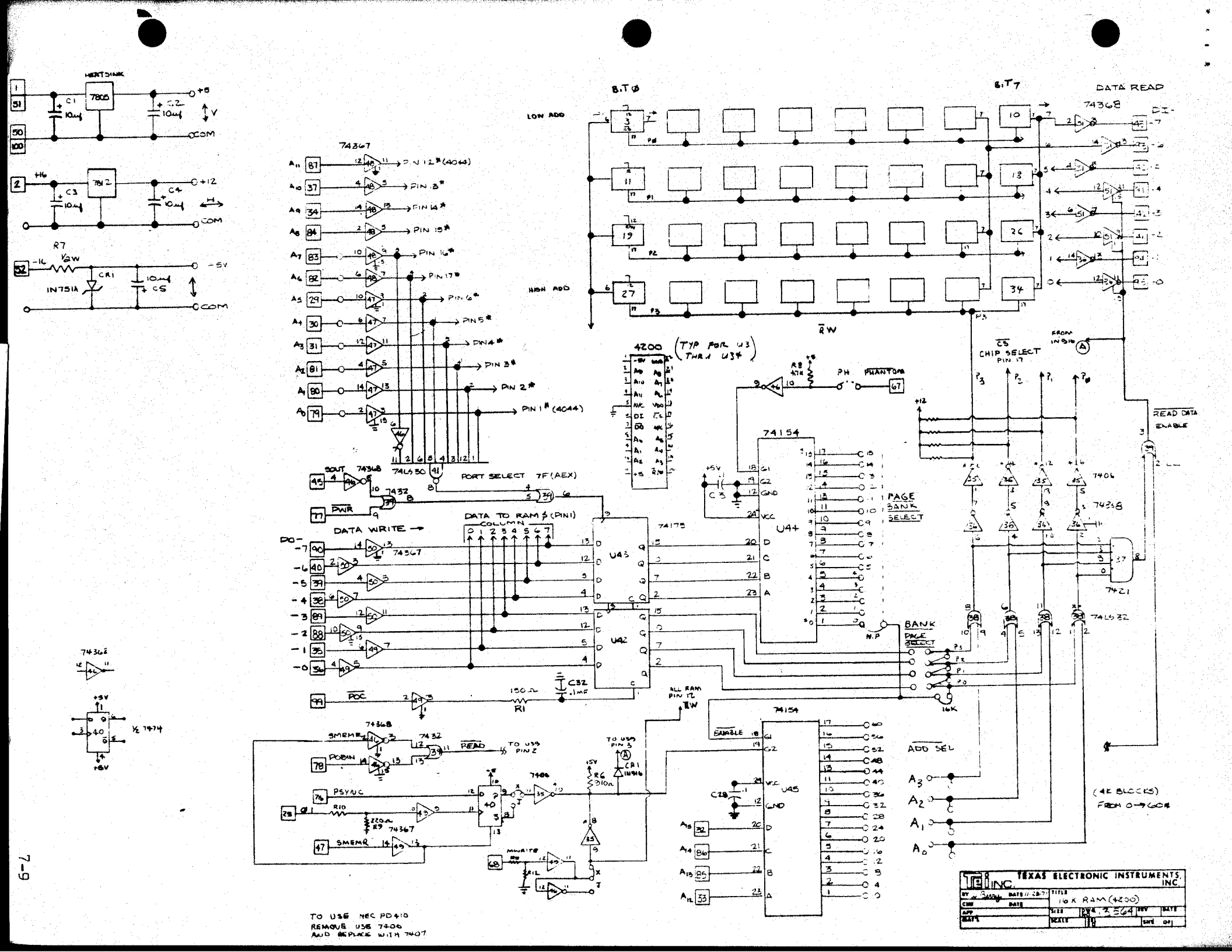
REF DES	DESCRIPTION	TEI P/N
C1 Thru C8	Cap 10MF, 20 VDC	1580-001
C9 Thru C32	Cap, .1MF	1562-002
R1	RES 150 Ω 1/4 W 2%	4741-258
U1 Thru U4	Regulator 7805	3120-003
U5 Thru U36	IC Chip RAM 6104-4	3163-009
U37	IC Chip 74LS367	3164-028
U38	IC Chip 74LS21	3164-026
U39, U44	IC Chip 74LS32	3164-027
U40	IC Chip 74LS30	3164-005
U41, U42	IC Chip 74LS175	3164-016
U43, U45	IC Chip 74LS154	3164-008
U46	IC Chip 74LS368	3164-029
U47 Thru		
U51	IC Chip 74LS367	3164-028
	Heat Sink, Regulator	4890-003
	PCB FAB.	13351

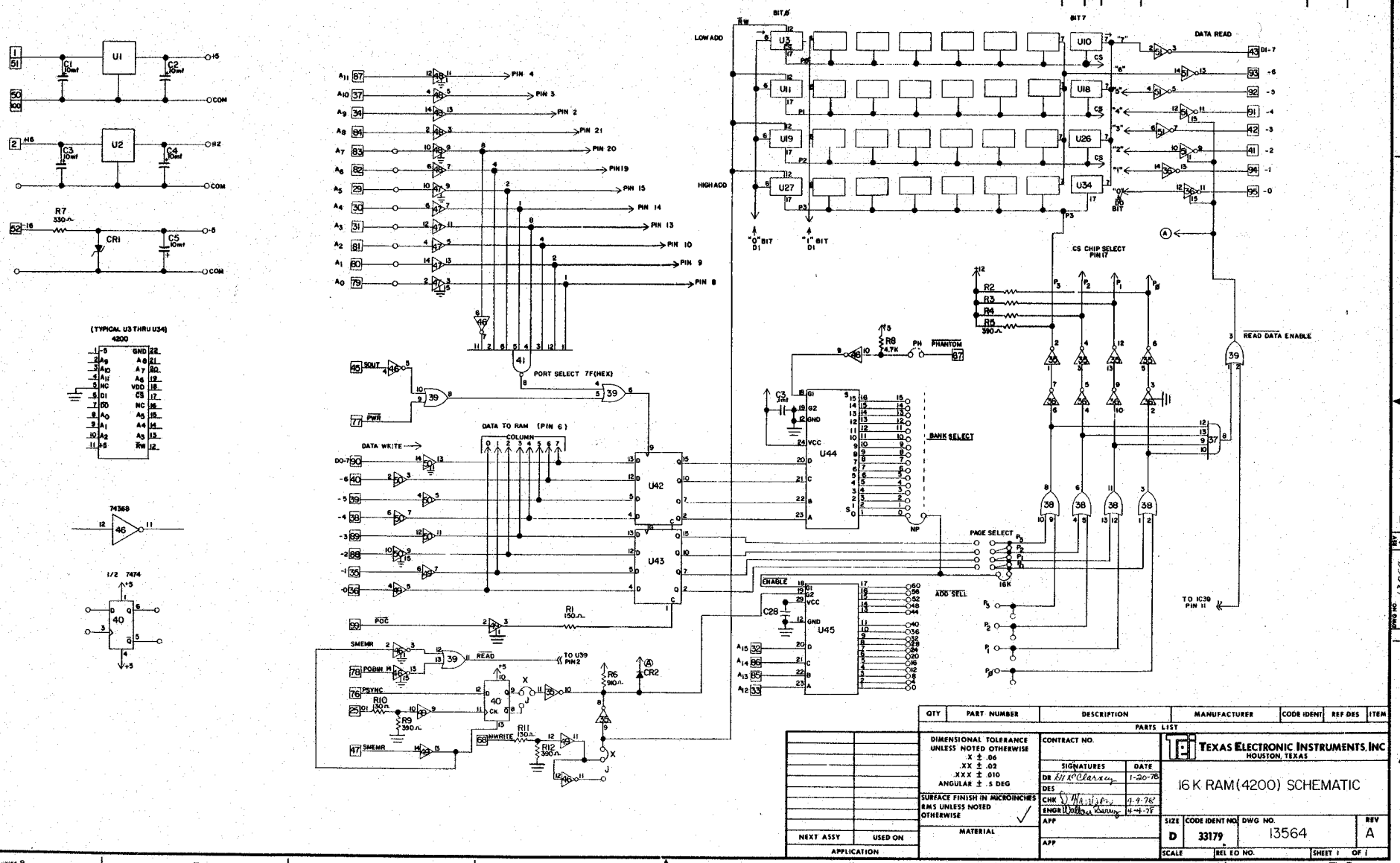
MCS- RAM 16K (4200) COMPONENT LAYOUT



MCS-RAM 16K (6104) COMPONENT LAYOUT




HEATSINK
7805
C1 10uf
C2 10uf
+5
V
COM
7812
C3 10uf
C4 10uf
+12
H
COM
R7 1/2W
CR1 IN751A
C5 10uf
-5V
COM
74367
PIN 12* (4044)
PIN 13*
PIN 14*
PIN 15*
PIN 16*
PIN 17*
PIN 6*
PIN 5*
PIN 4*
PIN 3*
PIN 2*
PIN 1* (4044)
74LS30
74368
SOUT
PWR
74LS32
PORT SELECT 7F(AEX)
DATA WRITE
DATA TO RAM (PIN1)
COLUMN
0 1 2 3 4 5 6 7
74175
U43
U42
74367
PDC
150Ω
R1
C32 .1MF
74368
SMEMR
74LS32
READ
TO U39 PIN 2
PDBIN
PSYNC
R10
220Ω R9
74367
SMEMR
MWRITE
R11
TO U39 PIN 3
R6 510Ω
CR1 IN916
7406
ALL RAM PIN 12
R/W
74154
U45
ENABLE
C29 .1
VCC
GND
A8
A14
A13
A12
74368
DATA READ
LOW ADD
HIGH ADD
B.T 0
B.T 7
DI-7
DI-6
DI-5
DI-4
DI-3
DI-2
DI-1
DI-0
P0
P1
P2
P3
R/W
4200 (TYP FOR U3 THRU U34)
R8 470
PH
PHANTOM
74154
U44
C3
PAGE BANK SELECT
N.P
BANK PAGE SELECT
16K
CS CHIP SELECT PIN 17
FROM IN516
READ DATA ENABLE
7406
74368
7421
74LS32
ADD SEL
A3
A2
A1
A0
(4K BLOCKS) FROM 0→60K
74368
+5V
½ 7474
TO USE NEC PD410
REMOVE U36 7406
AND REPLACE WITH 7407
TEXAS ELECTRONIC INSTRUMENTS, INC.
TITLE
16K RAM (4200)
SIZE
DWG 2564
REV
SHT 001


REVISIONS
ZONE | LTR | EO NO. | DESCRIPTION | DATE | APPROVED
A | 1034 | CORRECTED PIN NUMBERING | 8-9-78 | EME
U1
U2
C1 10mf
C2 10mf
C3 10mf
C4 10mf
C5 10mf
R7 330Ω
CR1
+5
COM
+12
-5
(TYPICAL U3 THRU U34)
4200
74368
1/2 7474
LOW ADD
HIGH ADD
BIT 0
BIT 7
DATA READ
"0" BIT D1
"1" BIT D1
CS CHIP SELECT PIN 17
U3
U11
U19
U27
U10
U18
U26
U34
R2
R3
R4
R5 390Ω
R6 4.7K
PH
PHANTOM
READ DATA ENABLE
BANK SELECT
PAGE SELECT
ADD SELL
TO IC39 PIN 11
U44
U45
U42
U43
C28
C3
PORT SELECT 7F(HEX)
DATA WRITE
DATA TO RAM (PIN 6)
COLUMN
R1 150Ω
R9 390Ω
R10 330Ω
R11 330Ω
R12 390Ω
R6 910Ω
CR2
TO U39 PIN 2
PIN 4
PIN 3
PIN 2
PIN 21
PIN 20
PIN 19
PIN 15
PIN 14
PIN 13
PIN 10
PIN 9
PIN 8
SOUT
PWR
POC
SMEMR
POBIN
PSYNC
MWRITE
READ
NOTES:
QTY | PART NUMBER | DESCRIPTION | MANUFACTURER | CODE IDENT | REF DES | ITEM
PARTS LIST
DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG
SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE
MATERIAL
NEXT ASSY | USED ON
APPLICATION
CONTRACT NO.
SIGNATURES | DATE
DR Bill Clarke | 1-20-78
DES
CHK | 4-9-78
ENGR | 4-4-78
APP
APP
TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS
16 K RAM (4200) SCHEMATIC
SIZE D | CODE IDENT NO. 33179 | DWG NO. 13564 | REV A
SCALE | REL EO NO. | SHEET 1 OF 1
DWG NO. 13564 REV A
7-9